Fig.1

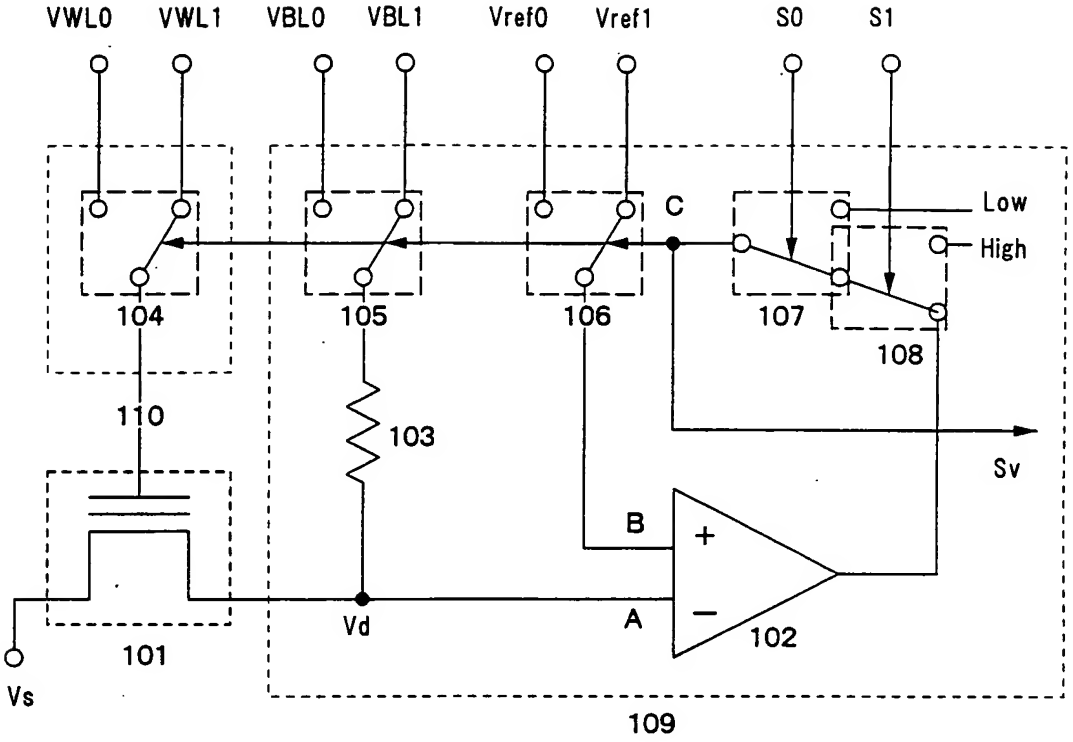
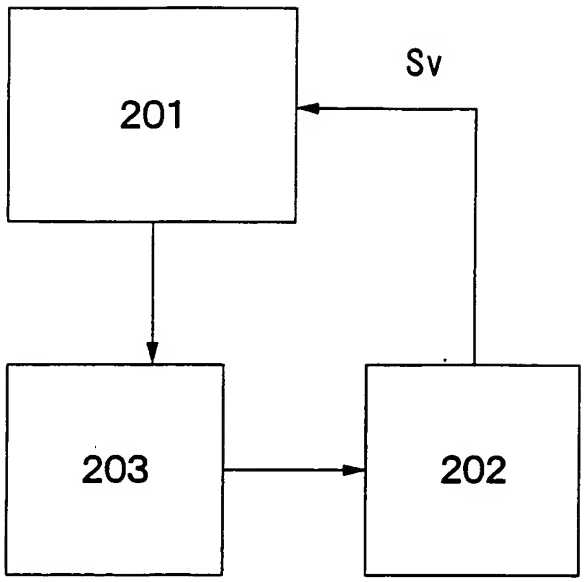

VWL0
VWL1
VBL0
VBL1
Vref0
Vref1
S0
S1
C
Low
High
104
105
106
107
108
110
103
Sv
B
+
A
−
102
Vd
101
Vs
109

Fig.2



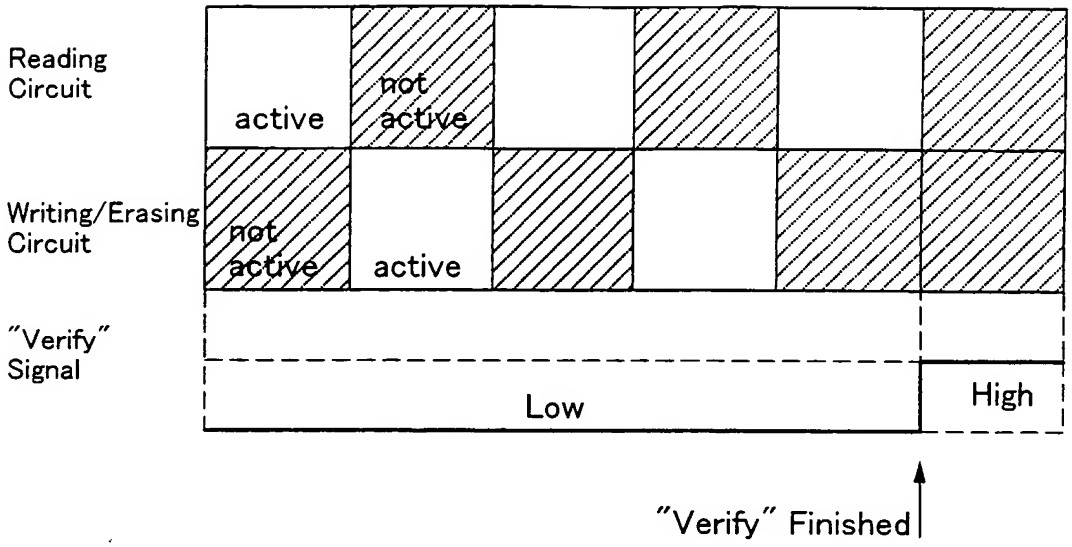

Reading Circuit
active
not active
Writing/Erasing Circuit
not active
active
"Verify" Signal
Low
High
"Verify" Finished

Fig.3

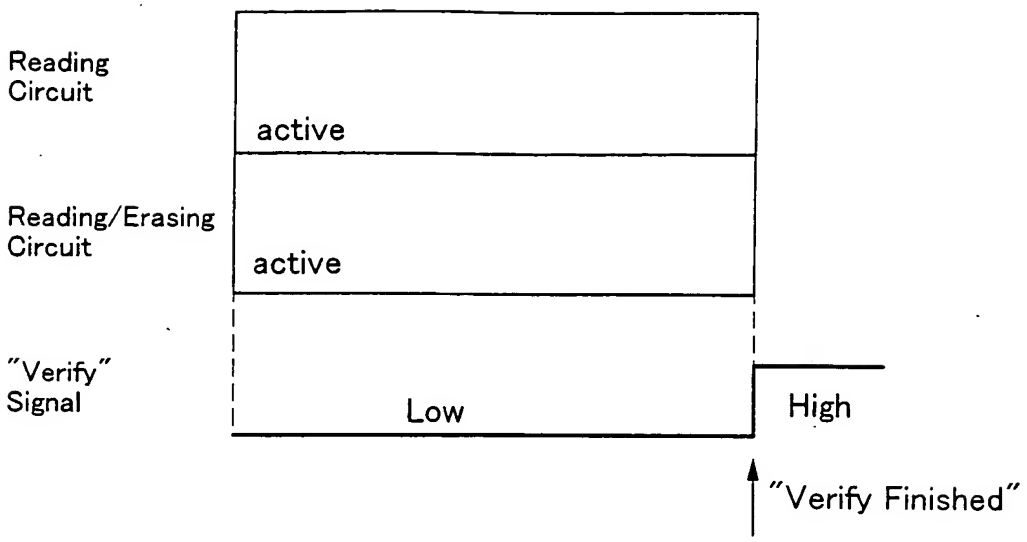

Reading
Circuit
active
Reading/Erasing
Circuit
active
"Verify"
Signal
Low
High
"Verify Finished"

Fig.4

Fig.5

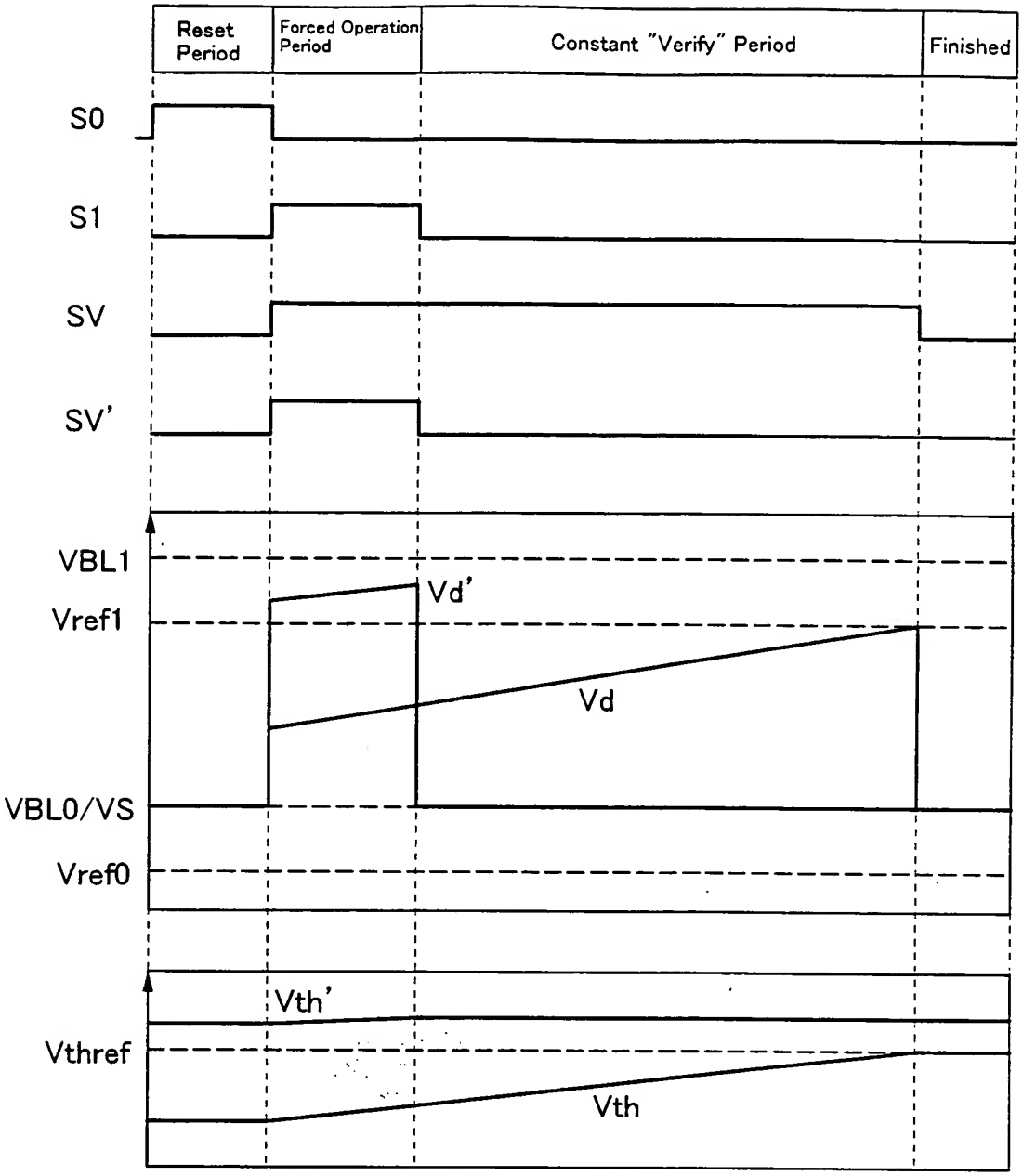

Reset Period
Forced Operation Period
Constant "Verify" Period
Finished
S0
S1
SV
SV'
VBL1
Vref1
Vd'
Vd
VBL0/VS
Vref0
Vth'
Vthref
Vth

Fig.6

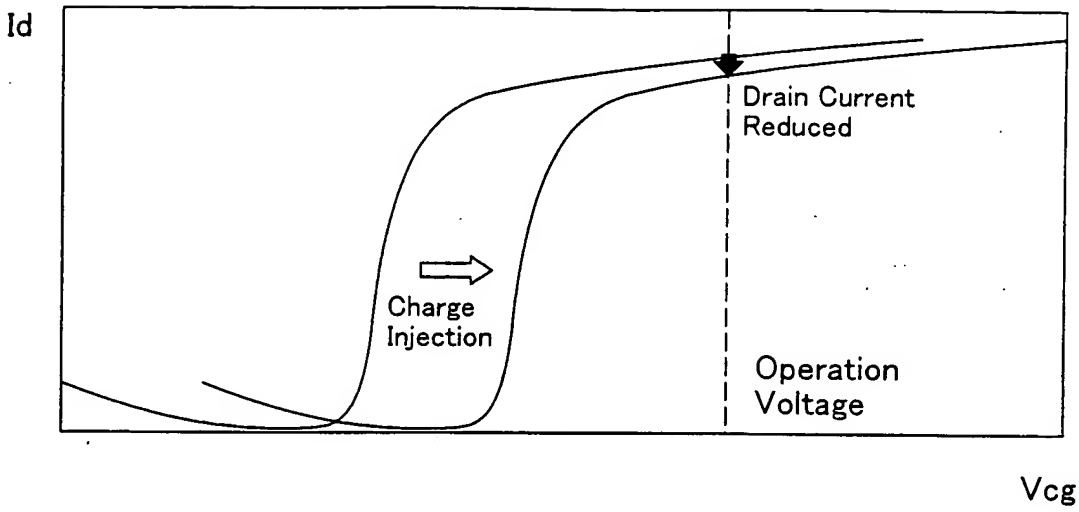

Id
Drain Current
Reduced
Charge
Injection
Operation
Voltage
Vcg

Fig.7

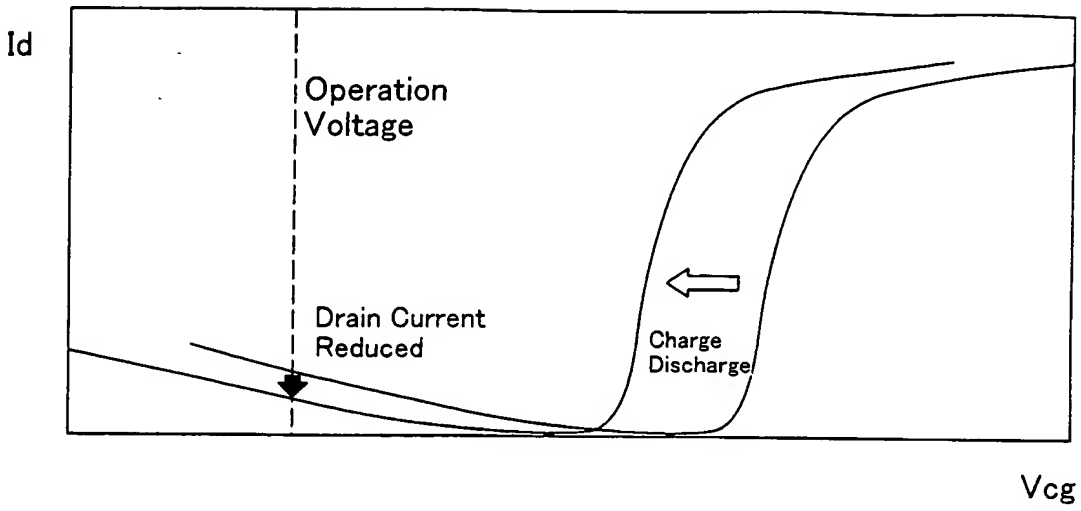

Id
Operation
Voltage
Drain Current
Reduced
Charge
Discharge
Vcg

Fig.8

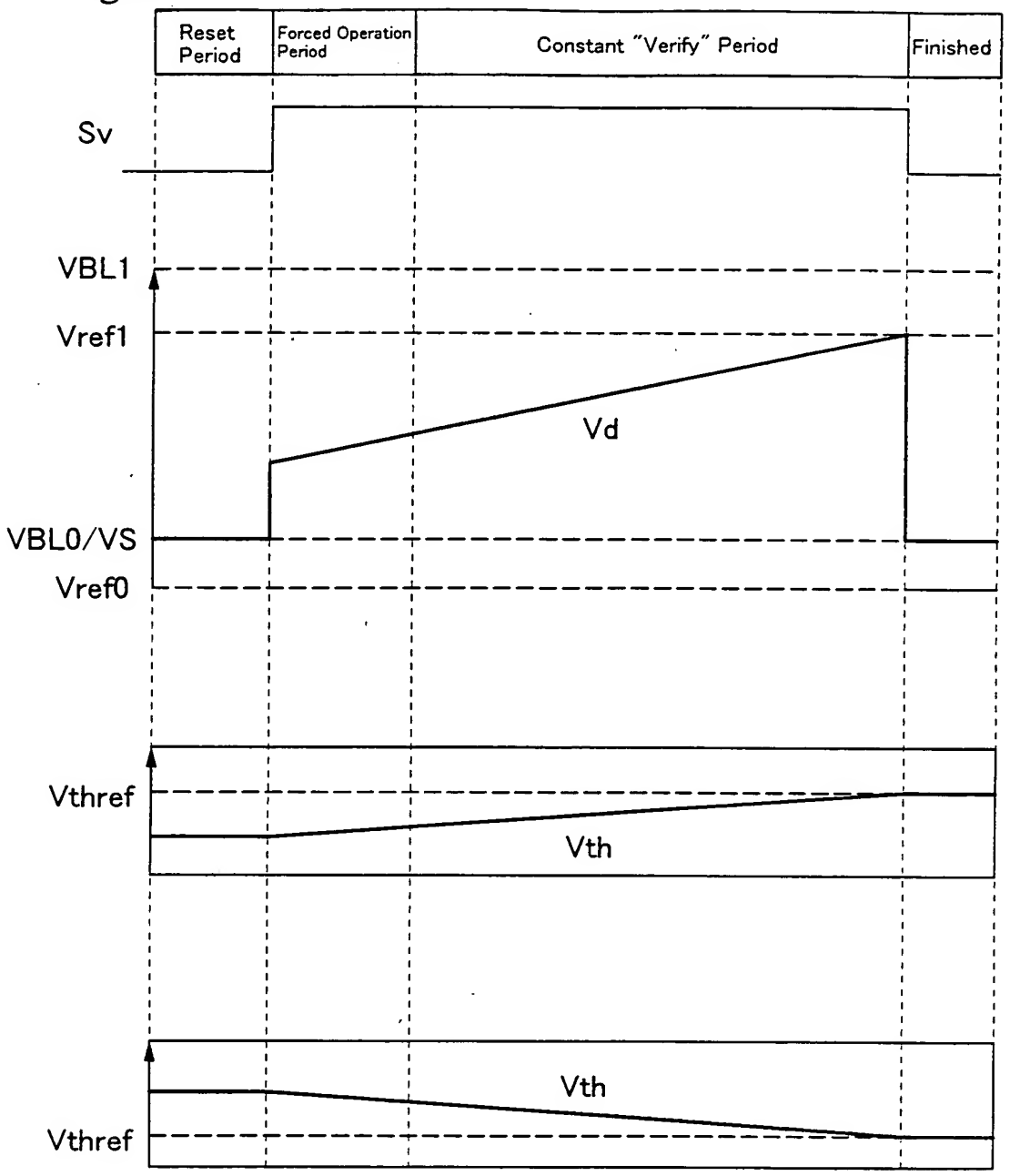

Reset Period
Forced Operation Period
Constant "Verify" Period
Finished
Sv
VBL1
Vref1
Vd
VBL0/VS
Vref0
Vthref
Vth
Vth
Vthref

Fig.9

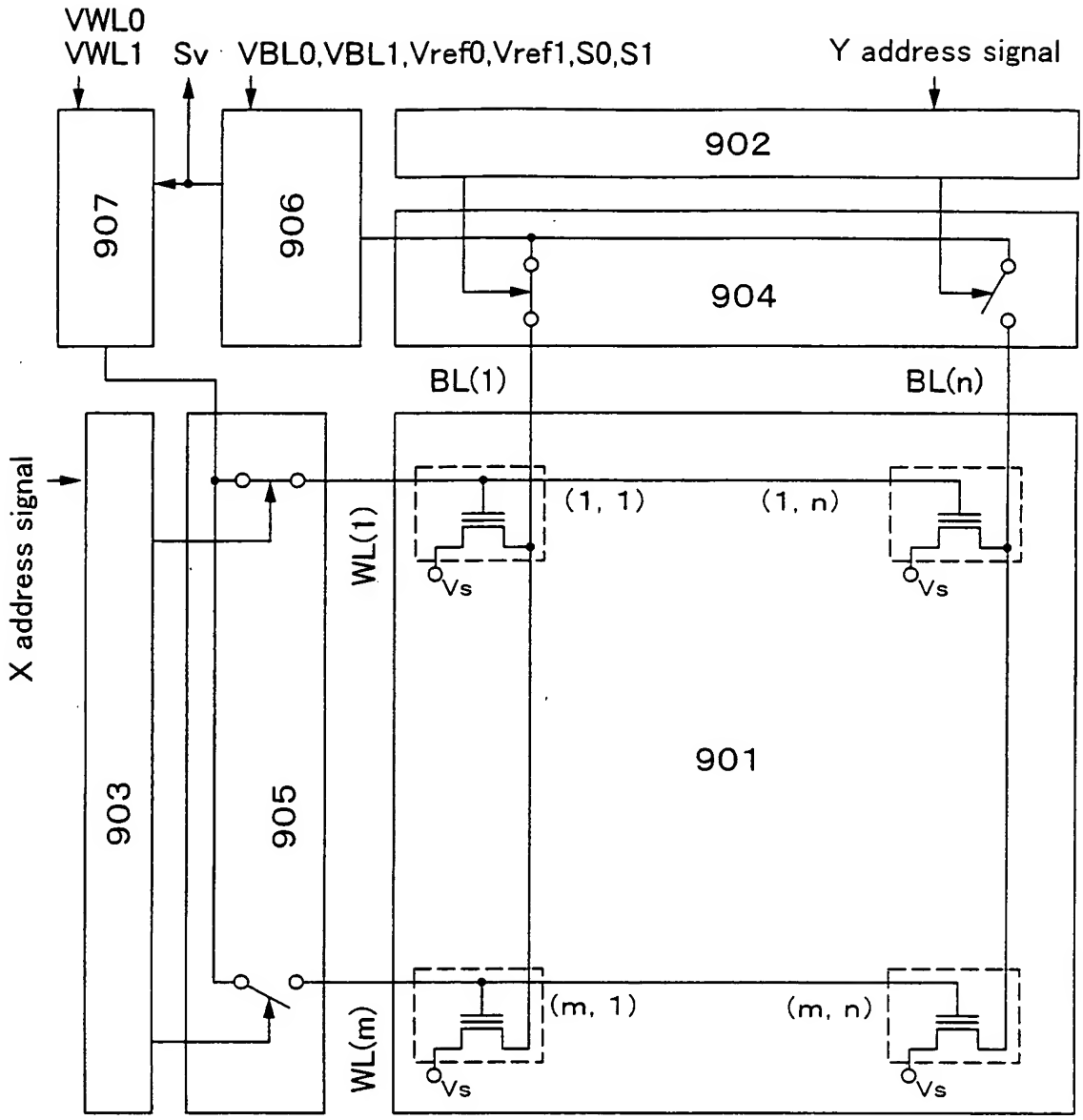

VWL0
VWL1
Sv
VBL0,VBL1,Vref0,Vref1,S0,S1
Y address signal
907
906
902
904
BL(1)
BL(n)
X address signal
903
905
WL(1)
WL(m)
(1, 1)
(1, n)
(m, 1)
(m, n)
Vs
901

Fig.10

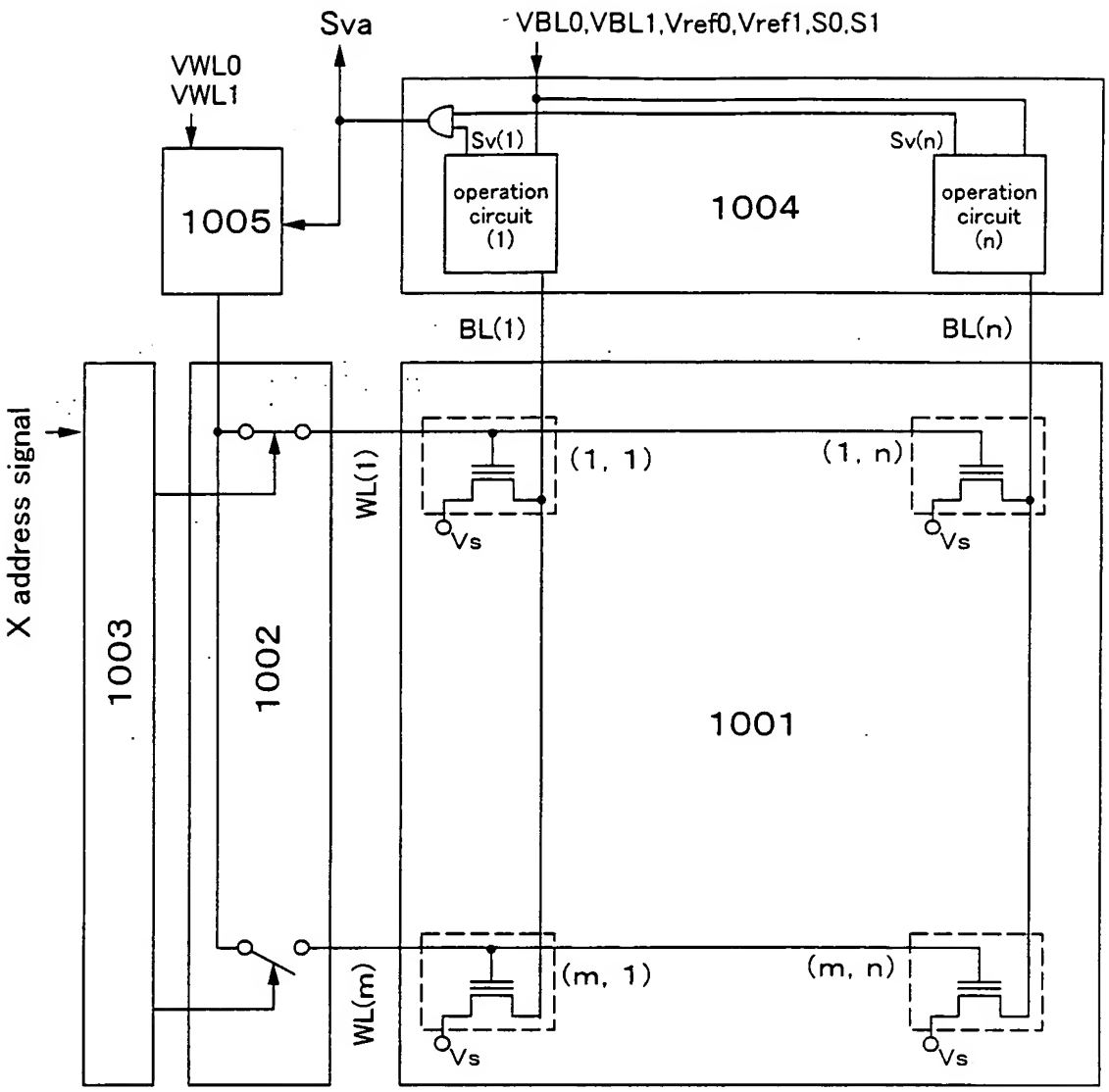

Sva
VBL0,VBL1,Vref0,Vref1,S0,S1
VWL0
VWL1
Sv(1)
Sv(n)
operation circuit (1)
operation circuit (n)
1004
1005
BL(1)
BL(n)
X address signal
1003
1002
1001
WL(1)
WL(m)
(1, 1)
(1, n)
(m, 1)
(m, n)
Vs

Fig.11

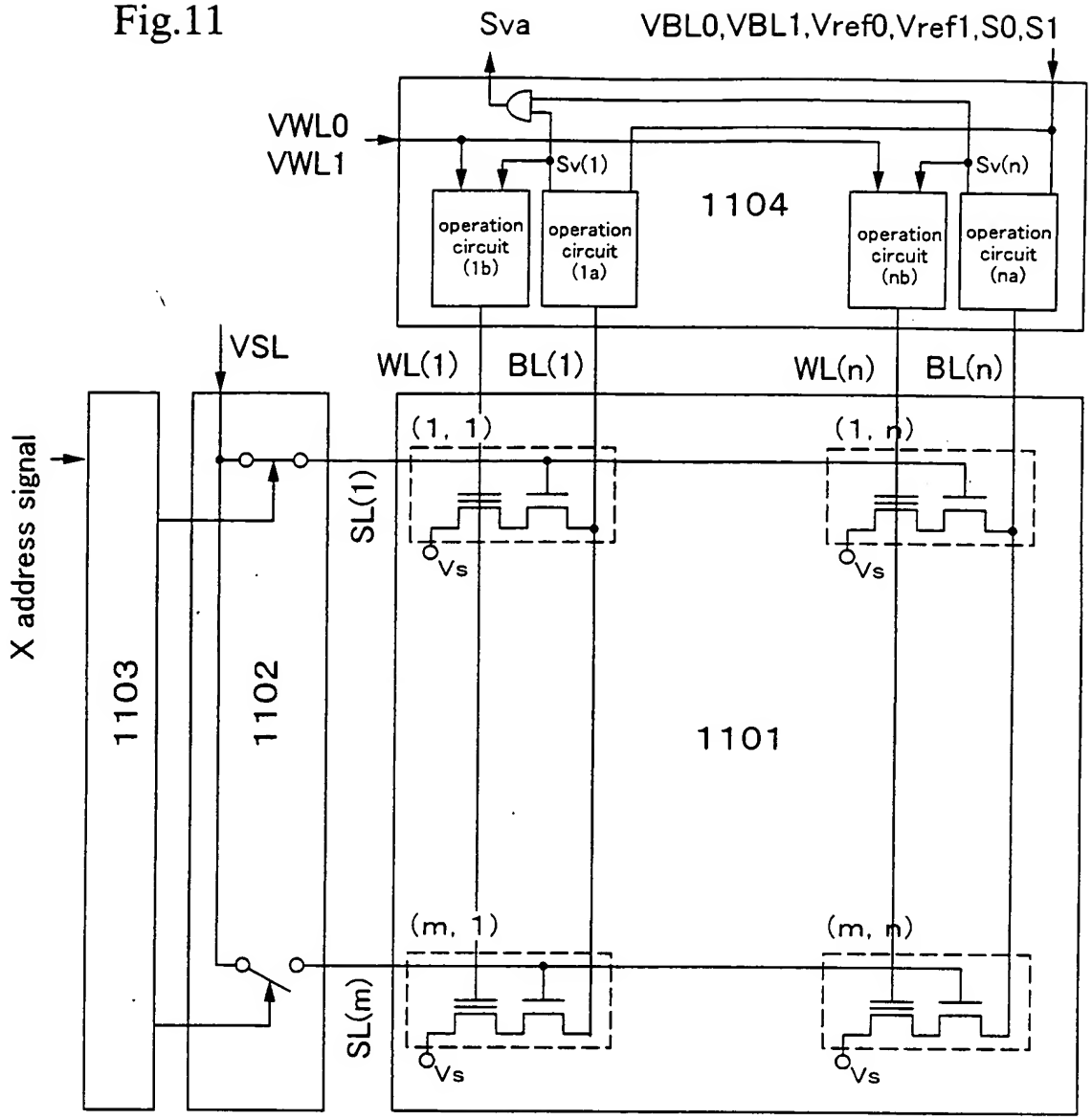

Sva
VBL0,VBL1,Vref0,Vref1,S0,S1
VWL0
VWL1
Sv(1)
Sv(n)
1104
operation circuit (1b)
operation circuit (1a)
operation circuit (nb)
operation circuit (na)
VSL
WL(1)
BL(1)
WL(n)
BL(n)
(1, 1)
(1, n)
SL(1)
Vs
X address signal
1103
1102
1101
(m, 1)
(m, n)
SL(m)

Fig.12

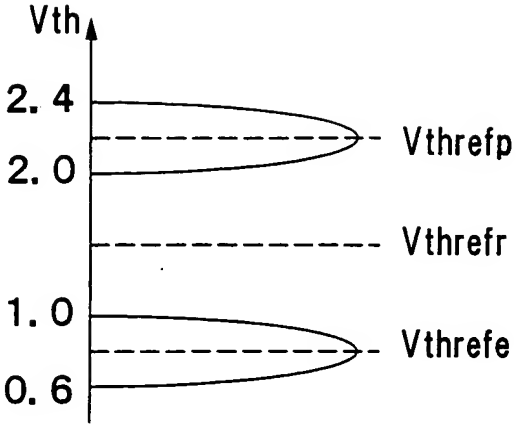


Fig.13A

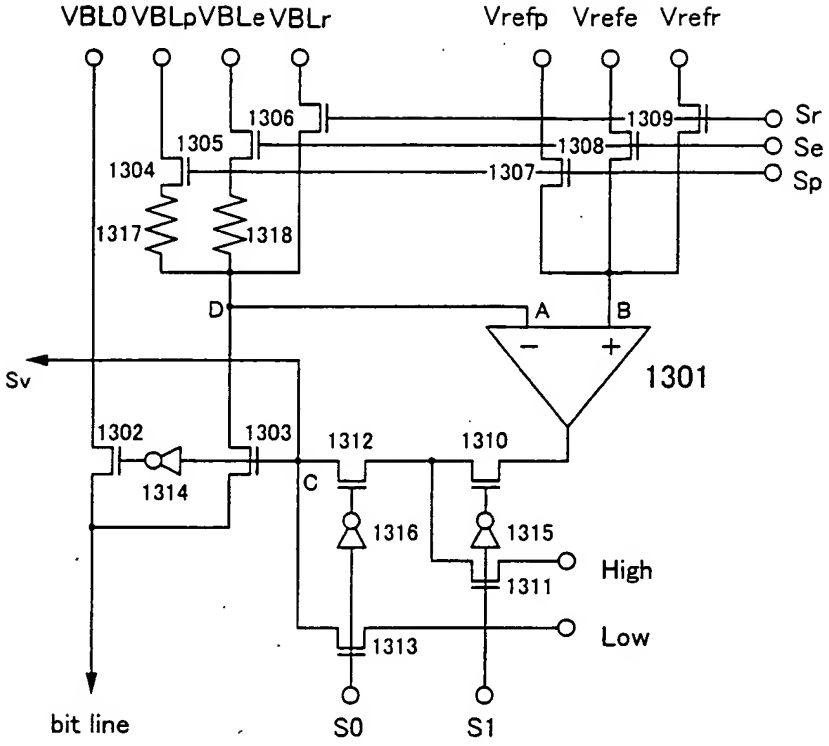


Fig.13B

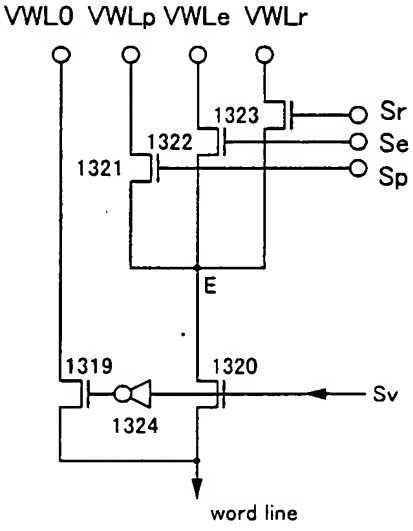


Fig.14A

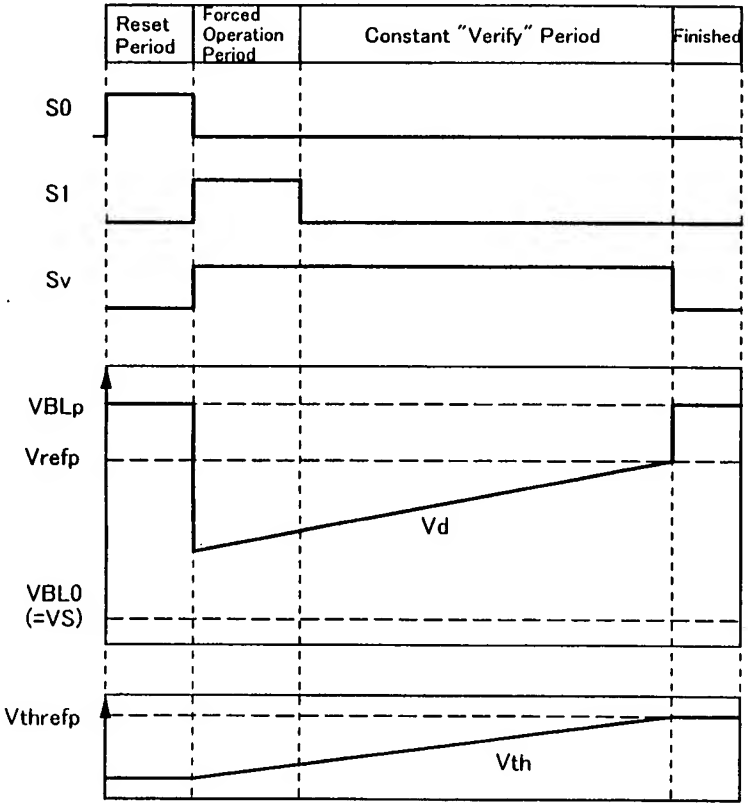


Fig.14B

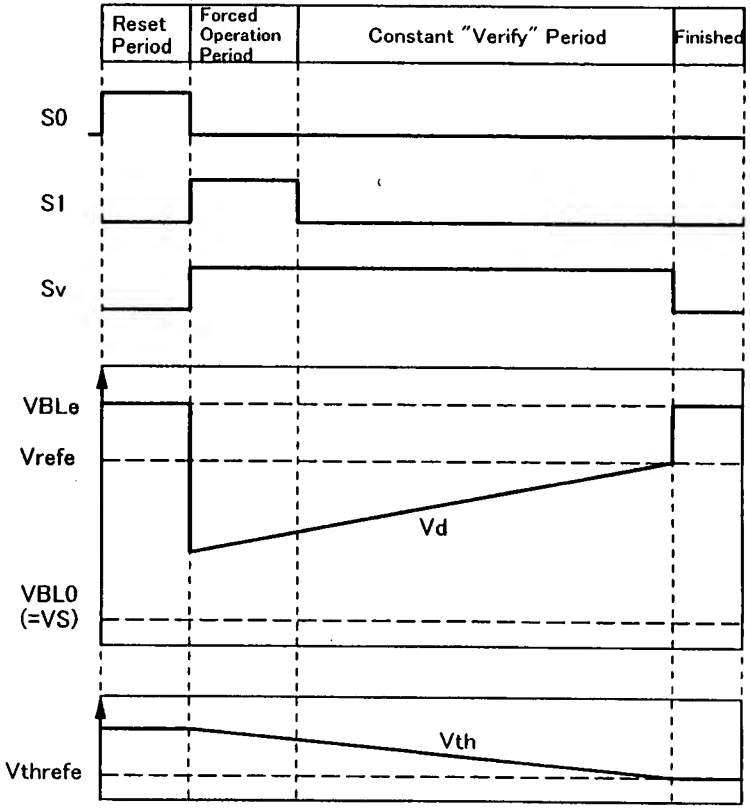
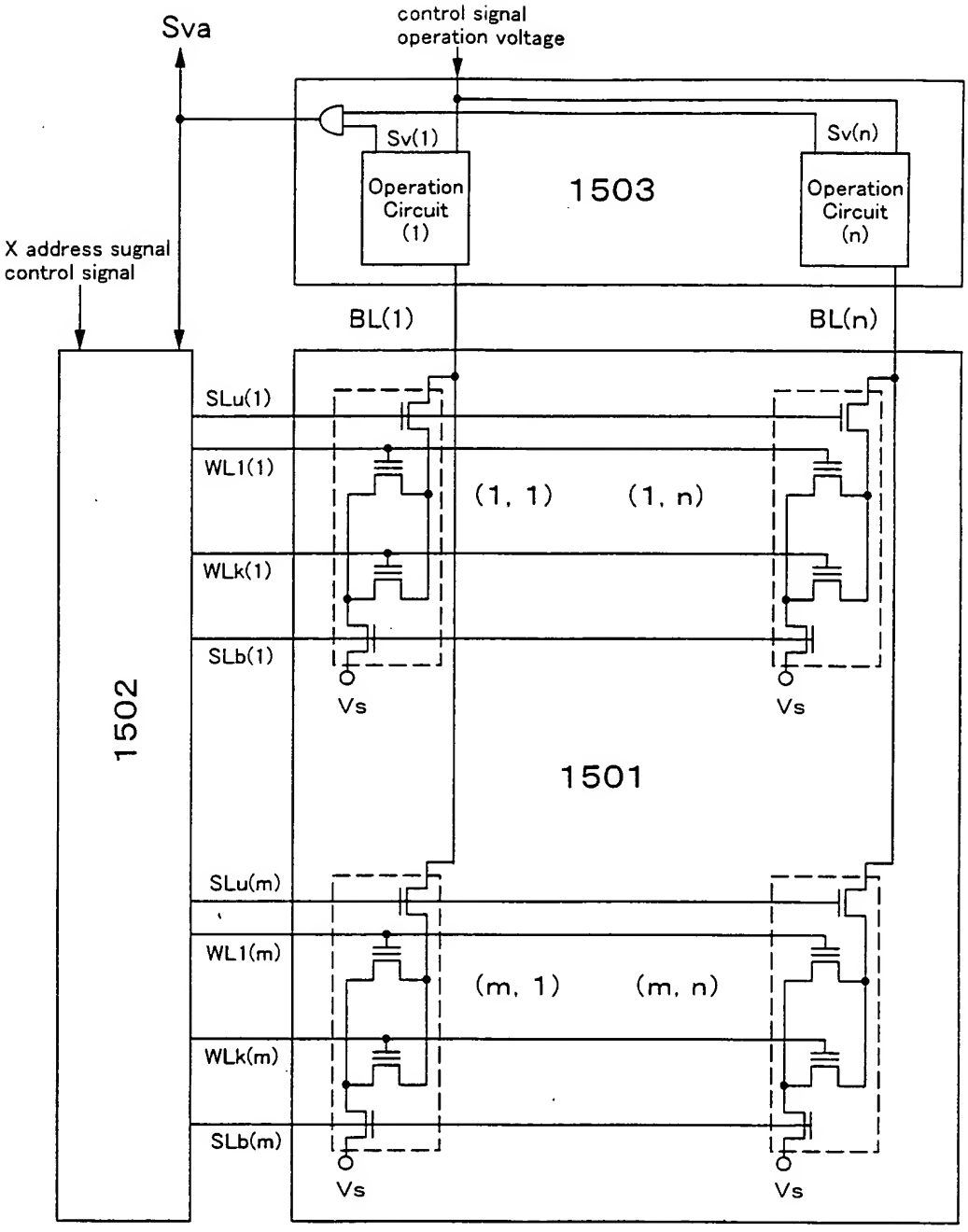


Fig.15


Sva
control signal
operation voltage
Sv(1)
Sv(n)
Operation Circuit (1)
1503
Operation Circuit (n)
X address sugnal
control signal
BL(1)
BL(n)
SLu(1)
WL1(1)
(1, 1)
(1, n)
WLk(1)
SLb(1)
Vs
Vs
1502
1501
SLu(m)
WL1(m)
(m, 1)
(m, n)
WLk(m)
SLb(m)
Vs
Vs

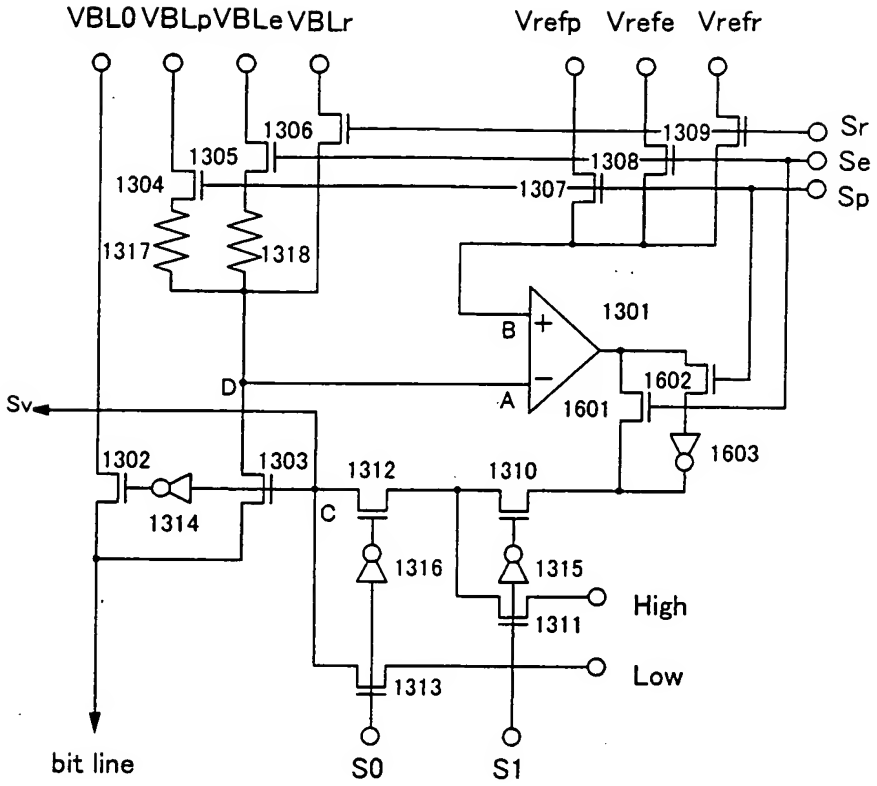

VBL0 VBLp VBLe VBLr
Vrefp Vrefe Vrefr
Sr
Se
Sp
1306
1309
1305
1308
1304
1307
1317
1318
1301
B
+
−
A
D
1602
1601
Sv
1603
1302
1303
1312
1310
1314
C
1316
1315
High
1311
Low
1313
bit line
S0
S1

Fig.16

Fig.17

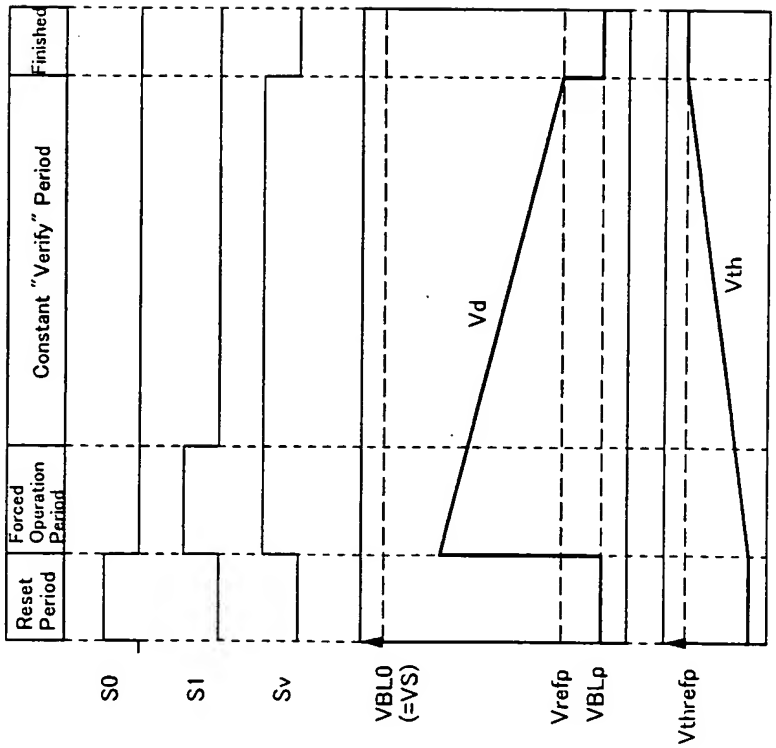

Reset Period
Forced Opuration Period
Constant "Verify" Period
Finished
S0
S1
Sv
VBL0 (=VS)
Vrefp
VBLp
Vthrefp
Vd
Vth

Fig.18

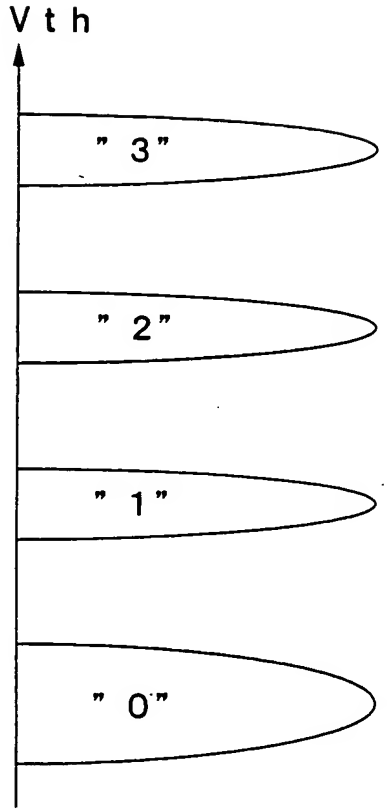
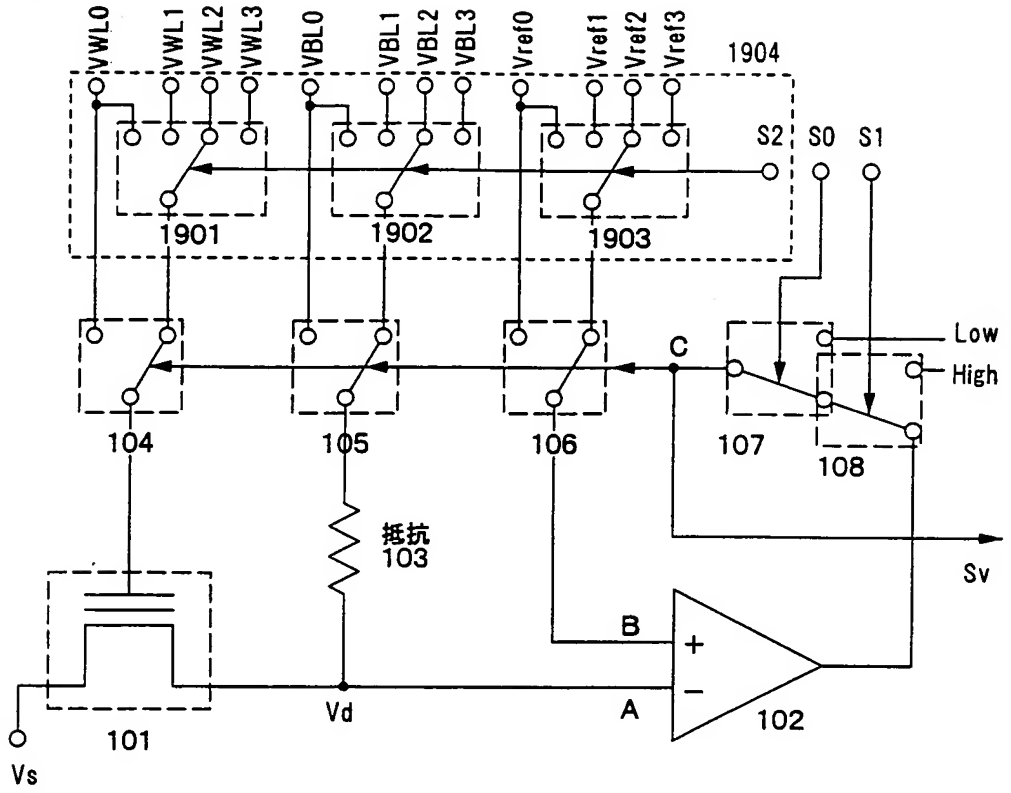


Fig.19


VWL0
VWL1
VWL2
VWL3
VBL0
VBL1
VBL2
VBL3
Vref0
Vref1
Vref2
Vref3
1904
S2
S0
S1
1901
1902
1903
Low
High
C
104
105
106
107
108
抵抗
103
Sv
B
A
Vd
101
102
Vs

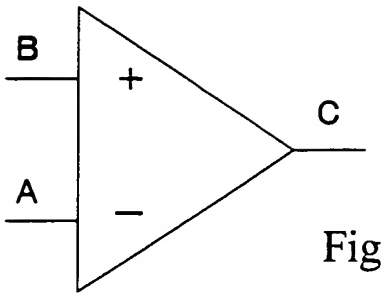


Fig.20A

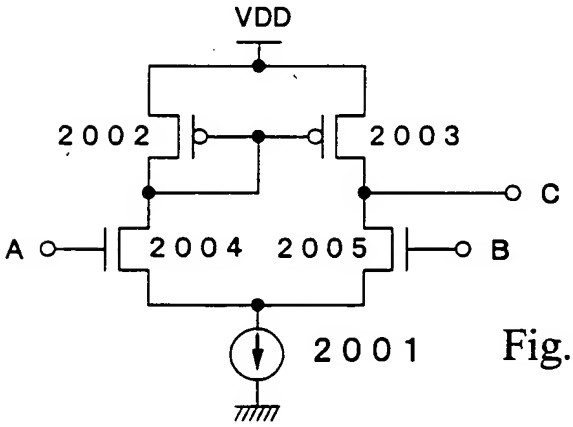
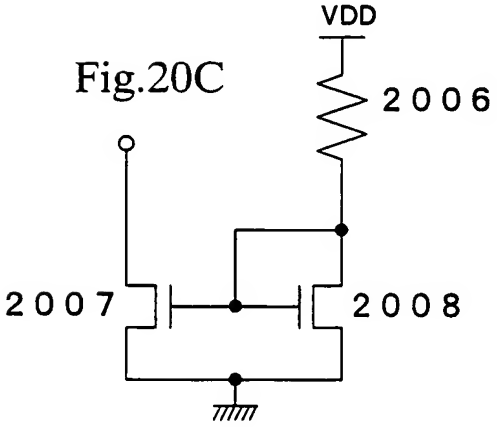


Fig.20B

Fig.20C



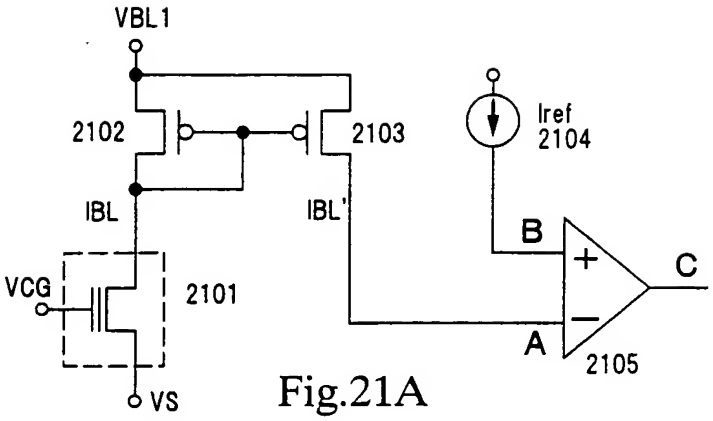


Fig.21A

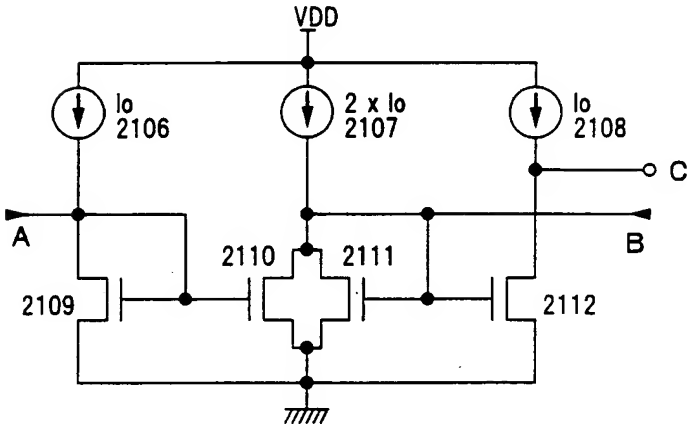


Fig.21B

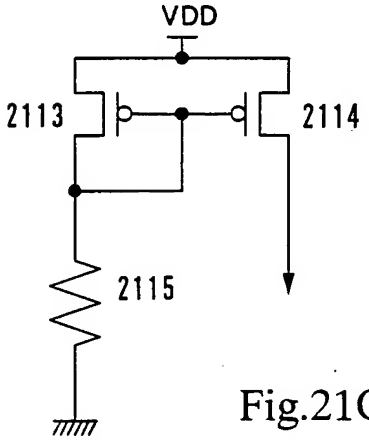


Fig.21C

Fig.22

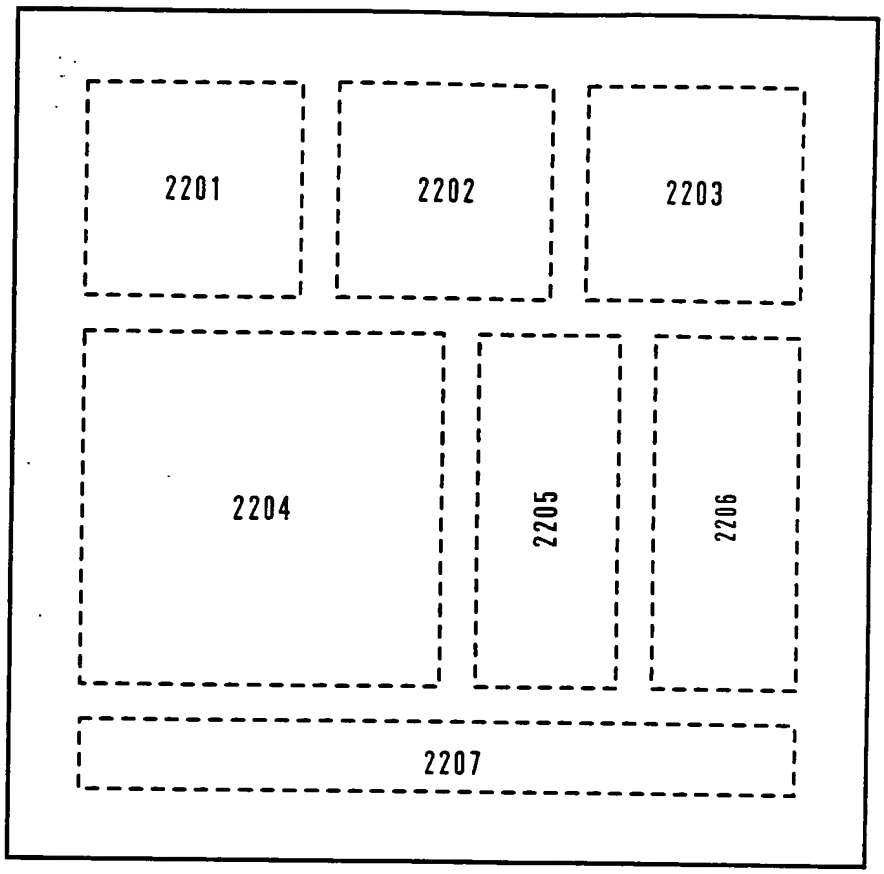


Fig.23

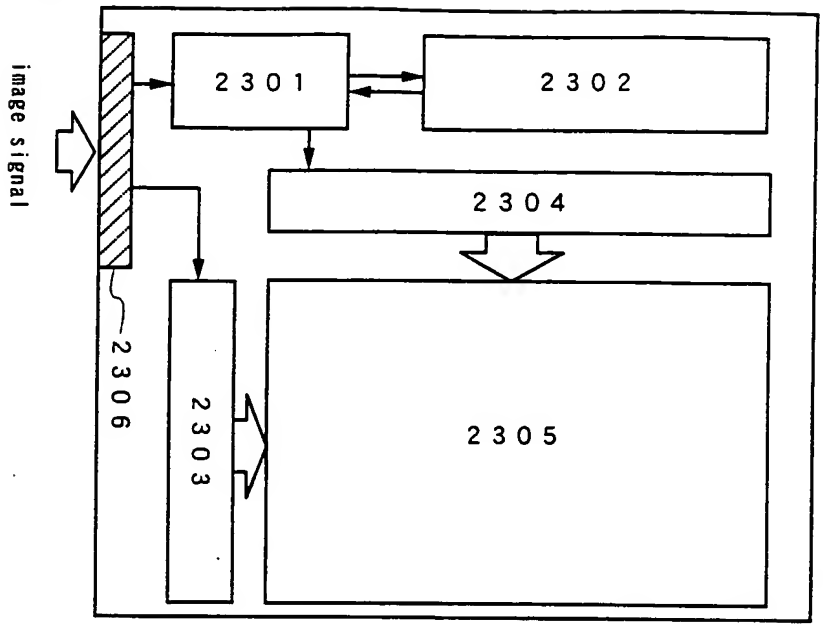


Fig.24

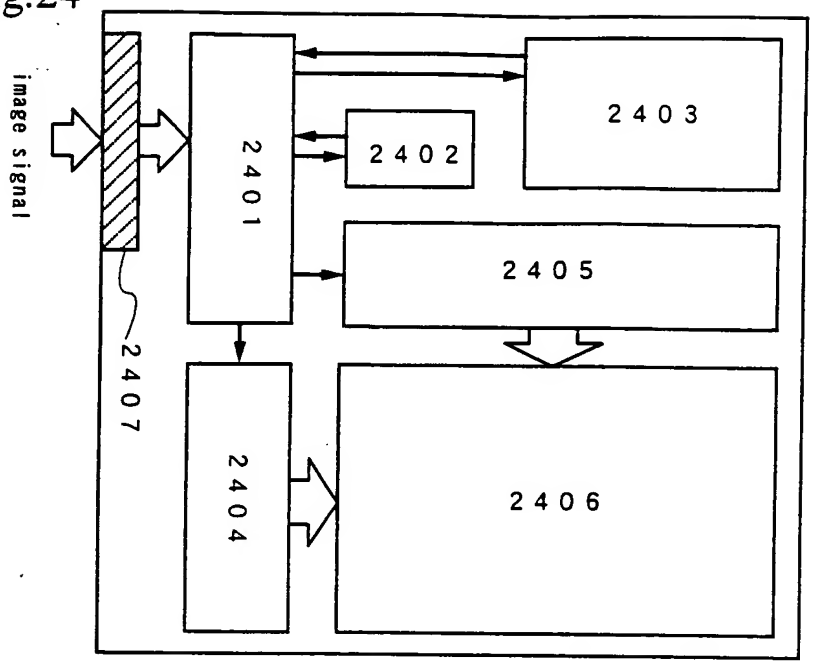
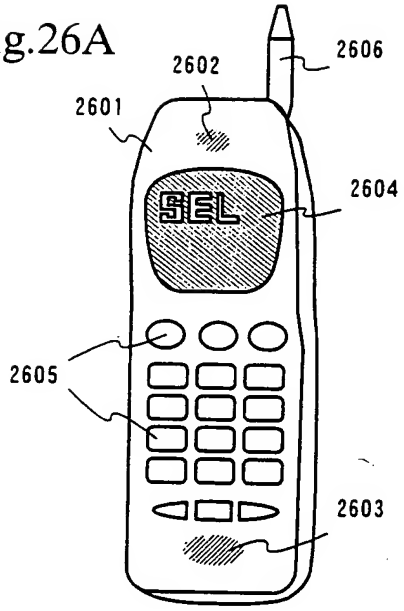


Fig.26A



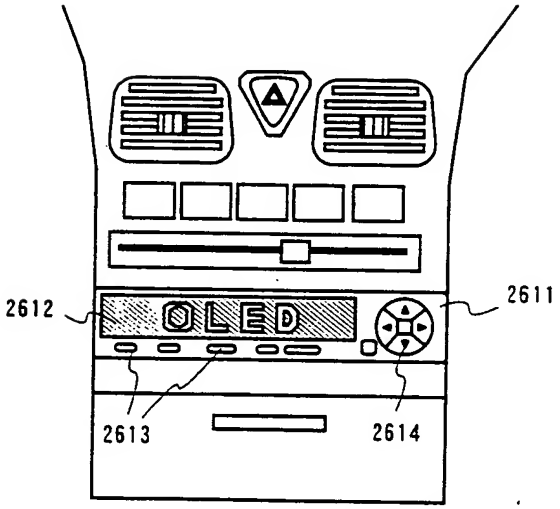


Fig.26B